CLAIMS

1. A surface channel MOSFET comprising:

a relaxed planarized SiGe layer on a substrate;

a regrown $Si_{1-x}Ge_x$ layer with thickness h;

a Si channel layer;

a gate dielectric;

a polycrystalline semiconductor layer; and

a highly conductive gate layer.

2. The MOSFET of claim 1, wherein h is approximately 0.

3. The MOSFET of claim 1, wherein the substrate comprises relaxed graded composition SiGe layers on Si.

4. The MOSFET of claim 1, wherein the substrate comprises Si.

5. The MOSFET of claim 1, wherein the substrate comprises Si with a layer of SiO_2.

6. A surface channel MOSFET comprising:

a relaxed planarized SiGe layer on a substrate;

a regrown $Si_{1-x}Ge_x$ layer with thickness h;

a Ge channel layer;

a Si layer;

a gate dielectric;

a polycrystalline semiconductor layer; and

a highly conductive gate layer.

7. The MOSFET of claim 6, wherein h is approximately 0.

8. The MOSFET of claim 6, wherein the thickness of the Si layer is less than 5nm.

9. The MOSFET of claim 6, wherein the substrate comprises relaxed graded composition SiGe layers on Si.

10. The MOSFET of claim 6, wherein the substrate comprises Si.

11. The MOSFET of claim 6, wherein the substrate comprises Si with a layer of SiO_2.

12. A buried channel MOSFET comprising:

a relaxed planarized SiGe layer on a substrate;

a regrown $Si_{1-x}Ge_x$ layer with thickness h;

a Si channel layer;

a $Si_{1-y}Ge_y$ layer;

a second Si layer;

a gate dielectric;

a polycrystalline semiconductor layer; and

a highly conductive gate metal layer.

13. The MOSFET of claim 12, wherein h is approximately 0.

14. The MOSFET of claim 12, wherein the thickness of the second Si layer is less than

2 5nm.

1 15. The MOSFET of claim 12, wherein supply layer dopants are located in the $Si_{1-y}Ge_y$
2 layer.

1 16. The MOSFET of claim 15, wherein the supply layer dopants are implanted.

1 17. The MOSFET of claim 12, wherein the supply layer dopants are located below the
2 Si channel layer.

1 18. The MOSFET of claim 17, wherein the supply layer dopants are implanted.

1 19. The MOSFET of claim 12, wherein the substrate comprises relaxed graded
2 composition SiGe layers on Si.

1 20. The MOSFET of claim 12, wherein the substrate comprises Si.

1 21. The MOSFET of claim 12, wherein the substrate comprises Si with a layer of
2 SiO_2.

1 22. A buried channel FET comprising:
2 a relaxed planarized SiGe layer on a substrate;
3 a regrown $Si_{1-x}Ge_x$ layer with thickness h;
4 a Si channel layer;
5 a $Si_{1-y}Ge_y$ layer;
6 a second Si layer; and

a highly conductive gate layer.

23. The FET of claim 22, wherein h is approximately 0.

24. The FET of claim 22, wherein the thickness of the second Si layer is less than 5nm.

25. The FET of claim 22, wherein supply layer dopants are located in the $Si_{1-y}Ge_y$ layer.

26. The FET of claim 25, wherein the supply layer dopants are implanted.

27. The FET of claim 22, wherein the supply layer dopants are located below the Si channel layer.

28. The FET of claim 27, wherein the supply layer dopants are implanted.

29. The FET of claim 22, wherein the substrate comprises relaxed graded composition SiGe layers on Si.

30. The FET of claim 22, wherein the substrate comprises Si.

31. The FET of claim 22, wherein the substrate comprises Si with a layer of SiO_2.